This listing of claims replaces all prior versions and listings of the claims in the application.

In the Claims

1. (currently amended) A conductor line stack, comprising:

a first layer consisting essentially of at least one first material selected from the group consisting of polysilicon and metal silicides;

a second layer consisting essentially of at least one second material formed on said first layer, said second layer having an upper portion and a lower portion;

an insulating cap overlying said second layer, said insulating cap having sidewalls aligned with sidewalls of said upper portion; and

a pair of first spacers disposed on sidewalls of said upper portion and on said aligned sidewalls of said insulating cap, said lower portion having width defined by a ~~combined~~ width of said upper portion combined with a width of ~~and~~ said pair of first spacers from said aligned sidewalls of said insulating cap.

2. (canceled)

3. (previously presented) The conductor line stack of claim 1, wherein said second material includes a metal.

4. (currently amended) The conductor line stack of claim 1, further comprising ~~an insulating cap disposed over said second layer, and~~ second spacers disposed on sidewalls of said first spacers, on sidewalls of said lower portion and on sidewalls of said first layer.

5. (original) A conductor contact structure including a conductor line stack as claimed in claim 4, further comprising a borderless bitline contact to a single-crystal

semiconductor region disposed below said conductor line stack, said bitline contact having a sidewall contacting a sidewall of said second spacer.

6. (previously presented) A conductor contact structure including a pair of conductor line stacks as claimed in claim 4, said conductor line stacks being oriented in parallel, said conductor contact structure including a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks, said bitline contact contacting sidewalls of said second spacers of said conductor line stacks.

7. (original) The conductor contact structure of claim 6 wherein said borderless bitline contact includes heavily doped polysilicon.

8. (canceled)

9. (previously presented) The conductor contact structure of claim 6 wherein a first conductor line stack of said pair of conductor line stacks is separated from said single-crystal semiconductor region by an array top oxide layer and a second conductor line stack of said pair of conductor line stacks is conductively coupled to a gate conductor of a vertical passgate transistor of a dynamic random access memory.

10. (currently amended) A conductor contact structure comprising:

a pair of conductor line stacks oriented in parallel, each said conductor line stack including:

a first layer consisting essentially of at least one first material selected from the group consisting essentially of doped polysilicon;

a second layer consisting essentially of at least one second material selected from the group consisting of metals and metal silicides overlying said first layer, said second layer having an upper portion and a lower portion;

an insulating cap ~~formed over~~ overlying said second layer, said insulating cap having sidewalls aligned with sidewalls of said upper portion; and

a pair of first spacers disposed on sidewalls of said upper portion and said insulating cap, said lower portion having width defined by a ~~combined~~ width of said upper portion combined with a width of~~and~~ said pair of first spacers from said aligned sidewalls of said insulating cap; and

a pair of second spacers disposed on sidewalls of said first spacers, on sidewalls of said lower portion and on sidewalls of said first layer;

a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks, said bitline contact contacting sidewalls of said second spacers of said conductor line stacks,

wherein a first conductor line stack of said pair of conductor line stacks is separated from said single-crystal semiconductor region by an array top oxide layer and a second conductor line stack of said pair of conductor line stacks is conductively coupled to a gate conductor of a vertical passgate transistor of a dynamic random access memory.

11-20. (canceled)

21. (currently amended) A conductor line stack, comprising:

a first layer consisting essentially of a doped polysilicon;

a second layer disposed on said first layer, said second layer consisting essentially of at least one second material selected from the group consisting of metals and conductive compounds of metals, said second layer having an upper portion and a lower portion;

an insulating cap overlying said second layer, said insulating cap having sidewalls aligned with sidewalls of said upper portion; and

a pair of first spacers disposed on sidewalls of said upper portion and on said aligned sidewalls of said insulating cap, said lower portion having width defined by a width of said upper portion combined with a width of said pair of first spacers from said aligned sidewalls of said insulating cap.

22. (currently amended) The conductor line stack of claim 21, further comprising ~~an insulating cap disposed over said second layer, and~~ second spacers disposed on sidewalls of said first spacers, on sidewalls of said lower portion and on sidewalls of said first layer.

23. (previously presented) A conductor contact structure including a conductor line stack as claimed in claim 22, further comprising a borderless bitline contact to a single-crystal semiconductor region disposed below said conductor line stack, said bitline contact having a sidewall contacting a sidewall of said second spacer.

24. (previously presented) A conductor contact structure including a pair of conductor line stacks as claimed in claim 22, said conductor line stacks being oriented in parallel, said conductor contact structure including a borderless bitline contact to a single-crystal semiconductor region disposed below said pair of conductor line stacks,

said bitline contact contacting sidewalls of said second spacers of said conductor line stacks.

25. (previously presented) The conductor contact structure of claim 24, wherein said borderless bitline contact includes doped polysilicon.

26. (previously presented) The conductor contact structure of claim 24, wherein a first conductor line stack of said pair of conductor line stacks is separated from said single-crystal semiconductor region by an array top oxide layer and a second conductor line stack of said pair of conductor line stacks is conductively coupled to a gate conductor of a vertical passgate transistor of a dynamic random access memory.

27. (new) The conductor line stack as claimed in claim 1 further comprising an etch stop layer disposed between said upper portion and said lower portion of said second layer, said etch stop layer including a third material which is substantially not attacked by an etchant which attacks said second material.

28. (new) The conductor contact structure as claimed in claim 10 further comprising an etch stop layer disposed between said upper portion and said lower portion of said second layer, said etch stop layer including a third material which is substantially not attacked by an etchant which attacks said second material.

29. (new) The conductor line stack as claimed in claim 21 further comprising an etch stop layer disposed between said upper portion and said lower portion of said second layer, said etch stop layer including a third material which is substantially not attacked by an etchant which attacks said second material.

30. (new) The conductor line stack as claimed in claim 1 further comprising an etch distinguishable layer disposed between said upper portion and said lower portion

of said second layer, said etch distinguishable layer including a third material which produces a chemical signal when contacted by an etchant which attacks said second material.

31. (new) The conductor contact structure as claimed in claim 10 further comprising an etch distinguishable layer disposed between said upper portion and said lower portion of said second layer, said etch distinguishable layer including a third material which produces a chemical signal when contacted by an etchant which attacks said second material.

32. (new) The conductor line stack as claimed in claim 21 further comprising an etch distinguishable layer disposed between said upper portion and said lower portion of said second layer, said etch distinguishable layer including a third material which produces a chemical signal when contacted by an etchant which attacks said second material.